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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/709,999 | 06/11/2004 | Michael C. Gaidis | FIS920040017US1 | 3998 |

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| EXAMINER | |
|---|---|
| LE, DUNG ANH | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/709,999 | GAIDIS ET AL. | |
| | Examiner | Art Unit | |
| | DUNG A. LE | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 20 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 June 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

***Oath/Declaration***

The oath/declaration filed on 6/11/2004 is acceptable.

***Election/Restriction***

Application's election **without traverse** of Group II (Claims 1-19) drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application . Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims.

Applicants are reminded to cancelled non-elective claims.

***Information Disclosure Statement***

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 10/27/2005 has/have been considered and made of record. The references cited on the PTOL 1449 form have been considered.

***Specification***

The specification is objected to for the following reason:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed (see MPEP § 606.01).

Note that, the claims are directed to a method of making a semiconductor device instead of to a semiconductor device.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## *Claim Rejections*

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1- 2, 10, 12-15 and 17 are rejected under 35 USC 102 (e) as being anticipated by Lee et al. (2005/0020076 A1).**

Lee et al. teach a method of patterning a magnetic tunnel junction (MTJ) stack (especially refer to figs. 2a-2b and related text) comprising:

forming an MTJ stack having a free layer 49 , a pinned layer45 and a tunnel barrier layer 47 disposed between said free layer and said pinned layer;

masking 53/51 a first area of said MTJ stack while exposing said free layer of said MTJ stack in a second area;

rendering said free layer electrically and magnetically inactive in said second area [0034].

**Regarding claim 2,** wherein said stack is formed over one or more interlevel dielectric layers 41 in which one or more respective metal conductor layers 43 are disposed .

**Regarding claim 10,** wherein said free layer is rendered electrically and magnetically inactive through oxidation [0033].

11. The method of claim 3, wherein said free layer is chemically altered by anodization.

**Regarding claim 12**, wherein said free layer is rendered electrically and magnetically inactive by physically 55 altering its composition ([0032] and fig. 2a).

**Regarding claim 13,** wherein said free layer is rendered electrically and magnetically inactive by adding additional atoms (implanting process 55 in fig. 2a) to said free layer.

**Regarding claim 14,** wherein the additional atoms are added by ion implantation (implanting process 55 in fig. 2a).

**Regarding claim 15**, wherein said free layer 19 [0013] includes a layer consisting essentially of nickel-iron (NiFe) .

**Claims 1, 3- 9, 12, 16 and 17 are rejected under 35 USC 102 (e) as being anticipated by Ying et al. (2004/0043526 A1).**

Ying et al. teach a method of patterning a magnetic tunnel junction (MTJ) stack (especially refer to figs. 2a- 2f and related text) comprising:

forming an MTJ stack having a free layer 206 , a pinned layer 210 and a tunnel barrier layer 208 disposed between said free layer and said pinned layer;

masking 230/240 a first area of said MTJ stack while exposing said free layer of said MTJ stack in a second area;

rendering said free layer 206 electrically and magnetically inactive in said second area 256 in fig. 2f.

**Regarding claim 3**, wherein said free layer is rendered electrically and magnetically inactive through conversion to an inert compound by chemically altering its composition [0029].

**Regarding claim 4**, wherein said free layer is chemically altered by plasma treatment [0019] and [0029].

**Regarding claim 5**, wherein said plasma treatment includes plasma oxidation [0019].

**Regarding claim 6,** wherein said plasma oxidation is performed at an elevated temperature that is higher than room temperature [0032].

**Regarding claim 7**, wherein said plasma oxidation is performed at a reduced temperature that is lower than room temperature [0032].

**Regarding claim 8,** wherein said chemical alteration further includes acceleration of oxygen ions [0029].

**Regarding claim 9**, wherein said free layer is chemically altered by exposure to a chemical agent including at least one agent selected from the group consisting of fluorine, carbon, and nitrogen [0029].

**Regarding claims 12 and 16**, wherein said free layer is rendered electrically and magnetically inactive by physically altering its composition and wherein the additional atoms are added by diffusion out of an adjacent "donor" film into said free layer of at least one agent selected from the group consisting of oxygen, nitrogen, fluorine, and carbon [0029].

**Regarding claim 17**, wherein said masking is conducted by forming a hardmask including at least one material selected from the group consisting of titanium nitride (TiN),

tantalum nitride (TaN), and a sacrificial material (fig.2E-2F and [0023]), wherein said free layer 206 includes iron ([0018] and [0021]), and said tunnel barrier layer 208 includes at least one material selected from the group consisting of aluminum oxide ([0018] and [0021) and magnesium oxide.

## Claim Rejections - 35 USC § 103

**The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:**

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claim 11 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Ying et al. in view of the following remark.**

Ying teaches the claimed invention as applied to claims 1 and 3 including the step of oxidizing the free layer using oxygen based plasma chemistry except for free layer is chemically altered by anodization as cited in current claim.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form free layer is chemically altered by anodization, because this process can be utilized to prevent undesirable or detrimental reactions in the contact region, since it has been held to be within the general skill of a worker in the art to select a known process on the basis of its suitability for the desired application.

**Set of claims18 -19**

**Claims 18- 19 are rejected under 35 USC 102 (e) as being anticipated by Lee et al. (2005/0020076 A1).**

Lee et al. teach a method of patterning an MTJ stack of a magneto-resistive random access memory (MRAM) comprising:

forming an interlevel dielectric layer 41 (ILD) over a substrate, said ILD including a plurality of conductive lines 43;

forming an MTJ stack overlying said ILD, said MTJ stack including a pinned layer 45, a tunnel barrier layer 47 overlying said pinned layer, and a free layer 49 overlying said tunnel barrier layer; masking 51/53 a portion of said MTJ stack to expose an area of said free layer; and converting said exposed area 49 of said free layer to a non-magnetic compound 57 by altering its composition (fig 2a-2b and related texts).

Lee does not disclose forming an interlevel dielectric layer 41 (ILD) over a substrate, said ILD including a plurality of vias.

Costrini et al. disclose the step of forming an interlevel dielectric layer (ILD) over a substrate, said ILD including a plurality of vias 6 [first right paragraph of page 4figs. 1- 4].

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form vias in Lee 's method in order to create the contacting for purpose of making electrical wiring between devices is made.

**Regarding claim 19,** wherein said exposed area is also rendered highly resistive 57 (fig. 2b and [0034].

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818